

In the Claims:

1. (Currently Amended) A transistor device comprising:
  - a semiconductor region having a top surface;
  - a source region in the semiconductor region;
  - a drain region in the semiconductor region;
  - a channel region in the semiconductor region between the source region and the drain region;
  - an impurity region within the channel region and spaced from the top surface, the impurity region having a first outer boundary that is proximate, but laterally spaced apart from the source region and a second outer boundary proximate, but laterally spaced apart from the drain region laterally spaced from the source and drain regions;
  - a gate overlying the channel region; and
  - a gate dielectric between the gate and the channel region.
2. (Original) The device of claim 1 wherein the semiconductor region comprises a region of monocrystalline silicon.
3. (Original) The device of claim 2 wherein the semiconductor region comprises a silicon substrate.
4. (Original) The device of claim 1 wherein the source and drain regions extend into the semiconductor region a first distance, and wherein the impurity region is spaced from the top surface by a distance less than the first distance.

5. (Original) The device of claim 1 wherein the gate dielectric comprises silicon dioxide.
6. (Original) The device of claim 1 wherein the impurity region comprises a region of an implanted oxygen bearing species in the channel region.
7. (Original) The device of claim 1 wherein the channel region comprises a strained channel region.
8. (Original) The device of claim 1 and further comprising:
  - a first sidewall spacer adjacent a first sidewall of the gate;
  - a second sidewall spacer adjacent a second sidewall of the gate;
  - a lightly doped drain region within the semiconductor region adjacent the drain region, the lightly doped drain region disposed beneath the first sidewall; and
  - a lightly doped source region within the semiconductor region adjacent the source region, the lightly doped source region disposed beneath the second sidewall.
9. (Original) The device of claim 1 and further comprising a second transistor, the second transistor including:
  - a second source region in the semiconductor region;
  - a second drain region in the semiconductor region;
  - a second channel region in the semiconductor region between the second source region and the second drain region;
  - a second gate overlying the channel region; and
  - a second gate dielectric between the gate and the channel region.

10. (Currently Amended) The device of claim 9 further comprising a second impurity region within the second channel region and spaced from the top surface, the second impurity region having a first outer boundary proximate, but laterally spaced apart from the source region and a second outer boundary that is proximate, but laterally spaced apart from the drain region ~~laterally spaced from the second source region and the second drain region.~~
11. (Original) The device of claim 9 wherein the second transistor does not include an impurity region within the second channel region.
12. (Original) The device of claim 9 wherein the second transistor device comprises an n-channel transistor.